

CLAIM LISTING:

1. (Currently Amended) A semiconductor device comprising:

an element substrate including a semiconductor layer of a first conductivity type being formed over a semiconductor substrate with a dielectric film interposed therebetween and such that said dielectric film is in contact with said semiconductor substrate;

said element substrate having a groove formed therein with a depth extending from a top surface of said semiconductor layer into said dielectric film, said groove ~~being formed to have an increased width portion~~ in said dielectric film, ~~said dielectric film of said increased width portion~~ being receded laterally as to expose a bottom surface of said semiconductor layer and such that the width of said groove in said dielectric film is greater than that of said groove in said semiconductor layer;

an impurity diffusion source buried in said ~~increased width~~ laterally receded portion of said groove to be contacted with ~~said bottom surface of said semiconductor layer~~ only said bottom surface in a whole surface of said semiconductor layer; and

a transistor having a first diffusion layer of a second conductivity type being formed through impurity diffusion from said impurity diffusion source to said bottom surface of said semiconductor layer, a second diffusion layer of the second conductivity type formed through impurity diffusion to said top surface of said semiconductor layer, and a gate electrode formed at a side face of said groove over said impurity diffusion source with a gate insulation film between said side face and said gate electrode.

2. (Previously Presented) The semiconductor device according to claim 1, wherein said groove is formed deep enough to reach the inside of said semiconductor substrate after penetration through said dielectric film, and further comprising:

a trench capacitor formed under said dielectric film to have a storage electrode as half buried in said groove, for constitution of a DRAM cell together with said transistor.

3. (Currently Amended) The semiconductor device according to claim 2, wherein a buried strap for use as said impurity diffusion source is formed and buried in said ~~increased width~~ laterally receded portion overlying said storage electrode to be contacted with said semiconductor layer only at the bottom surface thereof, and wherein this buried strap is covered with a cap insulation film with the gate electrode of said transistor embedded to overlie said cap insulation film.

4. (Currently Amended) The semiconductor device according to claim 3, wherein said buried strap comprises a first strap buried on said storage electrode and a second strap stacked on the first strap and buried in said ~~increased-width~~ laterally receded portion being in contact with said semiconductor layer only at the bottom surface thereof.

5. (Currently Amended) The semiconductor device according to claim 3, wherein said ~~increased-width~~ laterally receded portion of said groove is formed to cover an entire range of a thickness of said dielectric film whereas the storage electrode of said capacitor is half buried in said ~~increased-width~~ laterally receded portion with said buried strap being embedded on said storage electrode to be contacted with said semiconductor layer only at the bottom surface thereof.

6. (Previously Presented) The semiconductor device according to claim 2, wherein said semiconductor layer is partitioned into a plurality of element regions by an element isolating insulative film formed and buried deep enough to reach said dielectric film while letting two DRAM cells be disposed at opposite end portions of each said element region to thereby constitute a DRAM cell array with a word line connected to the gate electrode of said transistor and a bit line coupled to the second diffusion layer of said transistor said word line and said bit line being continuously disposed to cross each other.

7. (Previously Presented) The semiconductor device according to claim 6, wherein said bit line is in contact with said second diffusion layer of each DRAM cell at a position adjacent to word lines at both ends of each said element region, and wherein a body wire lead is formed to be contacted with said semiconductor layer across central part of said element region for applying a fixed potential to said semiconductor layer.

8. (Previously Presented) The semiconductor device according to claim 2, wherein said semiconductor layer is partitioned into a plurality of element regions by an element isolating insulative film formed and buried with a depth failing to reach said dielectric film while letting two DRAM cells be disposed at opposite end portions of each said element region to thereby constitute a DRAM cell array with a word line connected to the gate electrode of said transistor and a bit line coupled to the second diffusion layer of said transistor said word line and said bit line being continuously disposed to cross each other.

9 -20. (Cancelled)

21. (Currently Amended) A semiconductor device comprising:

an element substrate including a semiconductor layer of a first conductivity type being formed over a semiconductor substrate with a dielectric film interposed therebetween and such that said dielectric film is in contact with said semiconductor substrate;

said element substrate having a groove formed therein with a depth extending from a top surface of said semiconductor layer into the inside of said semiconductor substrate after penetration through said dielectric film, said groove ~~being formed to have an increased width portion in said dielectric film, said dielectric film of said increased width portion~~ being receded laterally as to expose a bottom surface of said semiconductor layer and such that the width of said groove in said dielectric film is greater than that of said groove in said semiconductor layer;

a trench capacitor formed under said dielectric film to have a storage electrode as half buried in said groove;

an impurity diffusion source buried in said ~~increased width~~ laterally receded portion of said groove to serve as a buried strap, bottom surface and top surface of said impurity diffusion source being contacted with said storage electrode and ~~said bottom surface of said semiconductor layer, respectively~~ only said bottom surface in a whole surface of said semiconductor layer, respectively;

a cap insulation film formed in said groove to cover said impurity diffusion source;
and

a transistor having a first diffusion layer of a second conductivity type being formed through impurity diffusion from said impurity diffusion source to said bottom surface of said semiconductor layer, a second diffusion layer of the second conductivity type formed through impurity diffusion to said top surface of said semiconductor layer, and a gate electrode formed at a side face of said groove over said impurity diffusion source with a gate insulation film between said side face and said gate electrode, said transistor constituting a DRAM cell with said trench capacitor.

22. (Previously Presented) The semiconductor device according to claim 21, wherein said buried strap comprises a first strap buried on said storage electrode and a second strap stacked on the first strap and buried in said increased width portion being in contact with said semiconductor layer only at the bottom surface thereof.

23. (Currently Amended) The semiconductor device according to claim 21, wherein said ~~increased width~~ laterally receded groove portion of said groove is formed to cover an entire range of a thickness of said dielectric film whereas the storage electrode of said capacitor as half buried in said increased width groove portion with said buried strap being embedded on said storage electrode to be contacted with said semiconductor layer only at the bottom surface thereof.

24. (Previously Presented) The semiconductor device according to claim 21, wherein said semiconductor layer is partitioned into a plurality of element regions by an element isolating insulative film as formed and buried deep enough to reach said dielectric film while letting two DRAM cells be disposed at opposite end portions of each said element region to thereby constitute a DRAM cell array with a word line connected to the gate electrode of said transistor and a bit line coupled to said second diffusion layer of said transistor, said word line and bit line being continuously disposed to cross each other.

25. (Previously Presented) The semiconductor device according to claim 24, wherein said bit line is in contact with said second diffusion layer of each DRAM cell at a position adjacent to word lines at both ends of each said element region, and wherein a body wire lead is formed to be contacted with said semiconductor layer across central part of said element region for applying a fixed potential to said semiconductor layer.

26. (Previously Presented) The semiconductor device according to claim 21, wherein said semiconductor layer is partitioned into a plurality of element regions by an element isolating insulative film as formed and buried with a depth failing to reach said dielectric film while letting two DRAM cells be disposed at opposite end portions of each said element region to thereby constitute a DRAM cell array with a word line connected to the gate electrode of said transistor and a bit line coupled to said second diffusion layer of said transistor, said word line and bit line being continuously disposed to cross each other.

27. (New) The semiconductor device according to claim 1, wherein said element substrate is a silicon-on-insulator substrate.

28. (New) The semiconductor device according to claim 21, wherein said element substrate is a silicon-on-insulator substrate.